IN THE SPECIFICATION

Please replace the Paragraph [0034] with the following paragraph:

[0034] Figure 3 illustrates a stacked chip-scale ball grid array package using memory dice according to one embodiment of the invention. A plurality of the chip-scale ball grid array packages 302 and 304 may be vertically stacked with a first surface of a first package 302 being coupled to an opposing second surface of a second package 304 and so on for each successive layer in the stack. In particular, the ~~solder balls 306~~ contact pads (e.g., 110 in Fig. 1) on the second surface of the second package 304 are electrically coupled to corresponding pads ~~(e.g., 110 in Fig. 1)~~ on the first surface of the first package 302. Because the solder balls ~~306~~ 308 have a larger vertical profile or height than the semiconductor die 305, this permits stacking the first package 302 over the second package 304. In this manner, a plurality of packages may be stacked to increase the density of semiconductor devices that may be mounted on a given area. For example, when the semiconductor die 301 and 305 are memory die, stacking a plurality of memory devices increases the capacity of a memory module in comparison to single-layer chip architectures.

Please replace the Paragraph [0035] with the following paragraph:

[0035] One aspect of the invention provides a chip-scale ball grid array package that permits mounting of components, such as capacitors and resistors, thereon. By mounting the semiconductor die 305 on the substrate 304 using connects 303, surface space is freed on the substrate above semiconductor die 305. In one implementation, the surface space above the semiconductor die always includes pads ~~308~~ 306 on which signal conditioning components may be mounted. This surface area may have one or more pads ~~308~~ 306 for connecting signal

filtering components thereon. This permits mounting on-chip electrical components 310, such as capacitors and resistors, which may be used for signal conditioning to and/or from the semiconductor die ~~301~~ 305. Being able to mount components 310 on the package substrate itself (e.g., chip-scale substrate) is an advantage over the prior art that was limited to mounting said components only external to the package. In one implementation ~~if~~ of the invention, such components 310 are signal conditioning capacitors and pull-up/pull-down resistors.

Please replace the Paragraph [0040] with the following paragraph:

[0040] Figure 6 illustrates a memory module 600 with a plurality of stacked memory components ~~602-612~~ 602, 604, 606, 608, 610, and 612 on both surfaces of the memory module 614 according to one embodiment of the invention. A plurality of stacked chip-scale ball grid array packages ~~602-612~~ 602, 604, 606, 608, 610, and 612 may be mounted on one or more surfaces of a substrate 614.

Please replace the Paragraph [0041] with the following paragraph:

[0041] In one implementation of the invention, the semiconductor devices (e.g., 102) may be random access memory devices mounted on stacked chip-scale packages (e.g., ~~602-612~~ 602, 604, 606, 608, 610, and 612). The stacked packages (e.g., ~~602-612~~ 602, 604, 606, 608, 610, and 612) are then mounted on either or both sides of a substrate to form a memory module 600, such as a single inline memory module (SIMM) or dual inline memory module (DIMM). The dimensional requirements of the memory module 600 may limit the number of packages (e.g., 100) that may be stacked.

Please replace the Paragraph [0046] with the following paragraph:

[0046] According to implementation of the novel routing scheme, each substrate ~~701~~ 701a-d includes a plurality of solder balls 705 mounted on a first surface of the substrate ~~701~~ 701a-d and a plurality of corresponding pads 707 on a second opposite surface of the substrate ~~701~~ 701a-d. Interconnects 709 serve to electrically couple the solder balls 705 to the pads 707. A cascading scheme, as illustrated in Fig. 7, permits independently accessing each semiconductor die from a primary access point (e.g., the solder balls on substrate 701a). The cascading scheme electrically couples the solder balls closest to the semiconductor die to a contact on the semiconductor die. For example, solder ball 711 is electrically coupled to a contact 702 on semiconductor die 703a. This implementation of the routing scheme provides for solder balls, on a first surface of a chip-scale package substrate, to be electrically coupled to pads, on a second surface of the chip-scale package substrate, that are closer to the semiconductor die. For example, solder ball 713 is electrically coupled to pad 715. Similarly, solder balls 717 and 719 are coupled to pads that are closer to the semiconductor die 703a. This routing scheme is implemented at every chip-scale package substrate 701a-d in the stack package 700. When the chip-scale package substrates are stacked on top of each other as shown, the each pad (e.g., 707) on the second surface of a first substrate (e.g., 701a) is electrically coupled to a corresponding solder ball (e.g., 720) on a first surface of a second substrate (e.g., 701b). Thus, a cascading routing scheme results that electrically couples solder balls (e.g., 713) in one substrate (e.g., 701a) to solder balls (e.g., 722) in a second substrate (e.g., 701b) that are closer to the interface point of a semiconductor die. Consequently, solder ball 713 is electrically coupled to connect 706, solder ball 717 is electrically coupled to connect 710, and solder ball 719 is electrically coupled to connect 714. A similar scheme may be implemented on the other side of the semiconductor die such that die

connects 704, 708, 712, and 716 are electrically coupled to solder balls on substrate 701a. The stacked package of semiconductor devices may then be coupled to another substrate or interface via the solder balls on the first surface of substrate 701a.